Silicon Nanotechnologies and Emerging Non-Si Nanoelectronics

Robert Chau

Intel Senior Fellow

Director of Transistor Research and Nanotechnology

Intel Corporation

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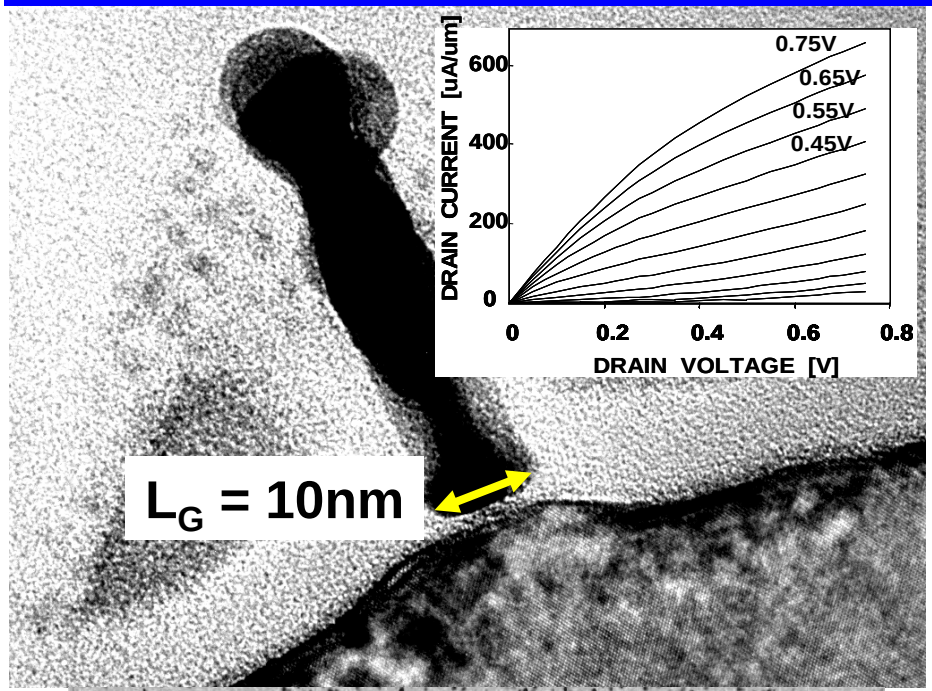
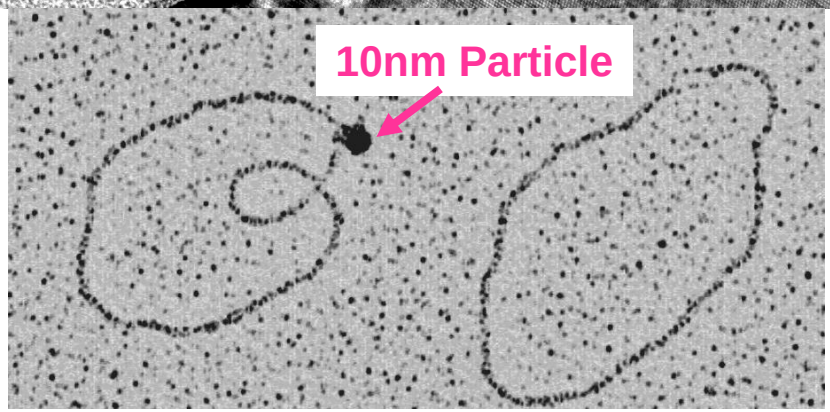
Content

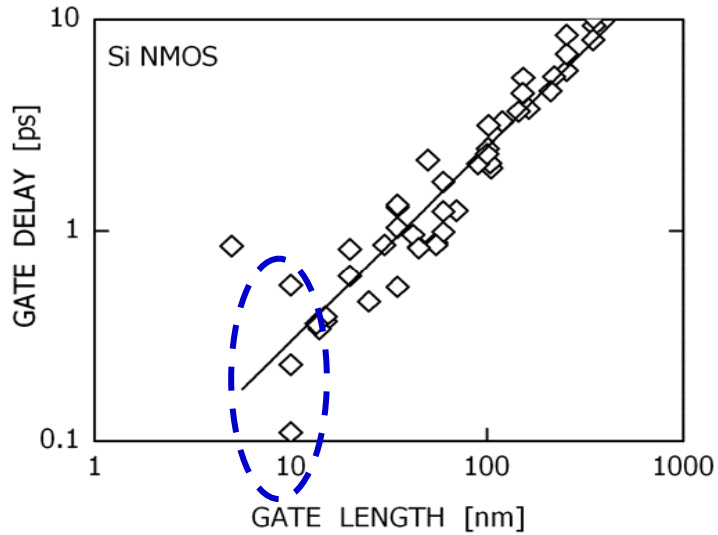
- State-of-the-art silicon innovations
- Emerging non-Si nanoelectronic devices
- Why III-V nanoelectronics research ?
- Performance of III-V quantum-well (QW) devices at ultra-low supply voltage (e.g. 0.5V)
- Challenges and opportunities
- Summary

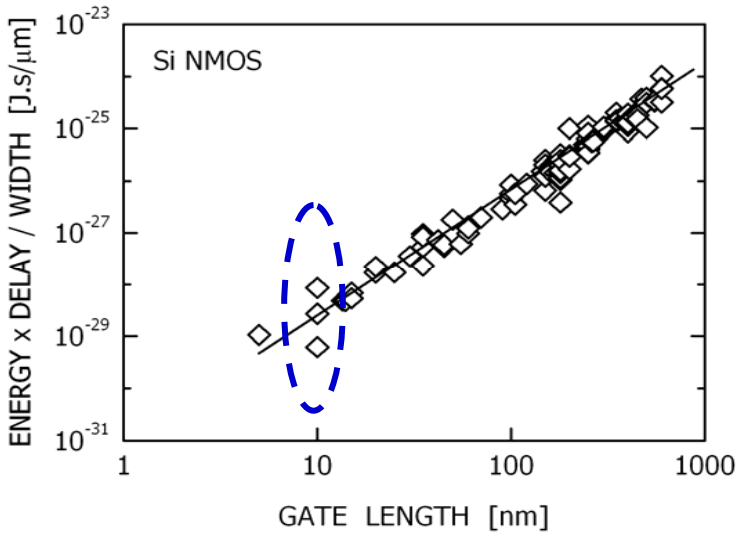
Silicon Transistor Scaling: Smaller than DNA





10nm Gold particle attached to Z-DNA antibody [Source: John Jackson & Inman, Gene 1989, 84 221-226]



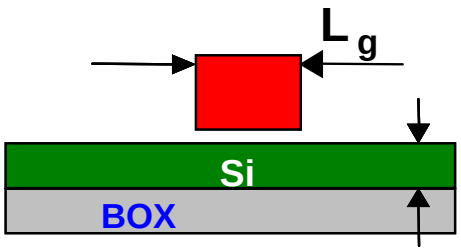


Source: R. Chau *et al.*, DRC 2003

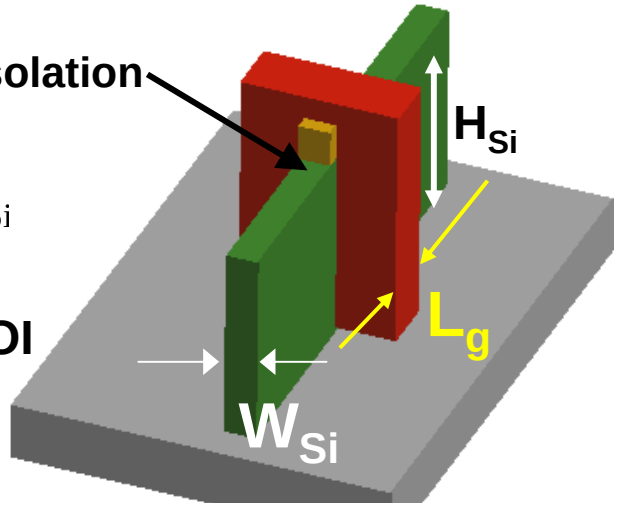
Examples of Recent Silicon Innovations

- **Strained Silicon**
  - P. Bai *et al*., IEDM 2004. S. Tyagi *et al*, IEDM 2005.
  - Implemented in Intel's 90nm and 65nm technology nodes.
- **FUSI metal-gate on thin SiO2**
  - P. Ranade *et al*., IEDM 2005.
- **High-K/Metal-Gate**
  - R. Chau *et. al.*, IWGI, Nov. 2003. R. Chau, AVS ICMI, Mar. 2004. R. Chau *et al*., IEEE EDL, Vol. 25, No. 6, pp.408 - 410, June 2004.
- **Non-planar fully-depleted Tri-gate transistor**
  - R. Chau *et. al*., SSDM 2002. B. Doyle, R.Chau *et al*., VLSI 2003.
- **Tri-gate transistors combined with i) strain, ii) high-K/metal-gate, and iii) dual epi raised source/drain**
  - J. Kavalieros *et al*., VLSI 2006.

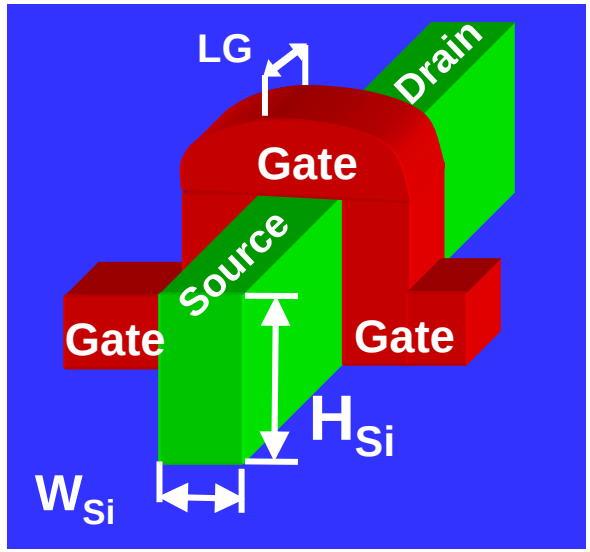
Device Structures to Improve Electrostatics



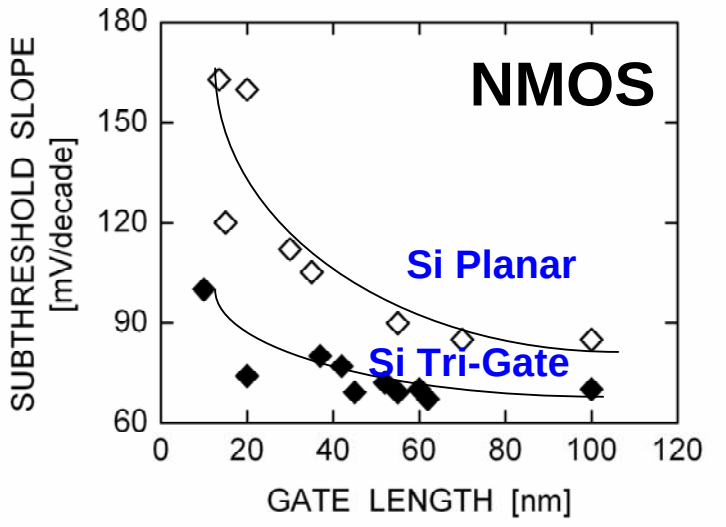
Planar Fully-Depleted SOI

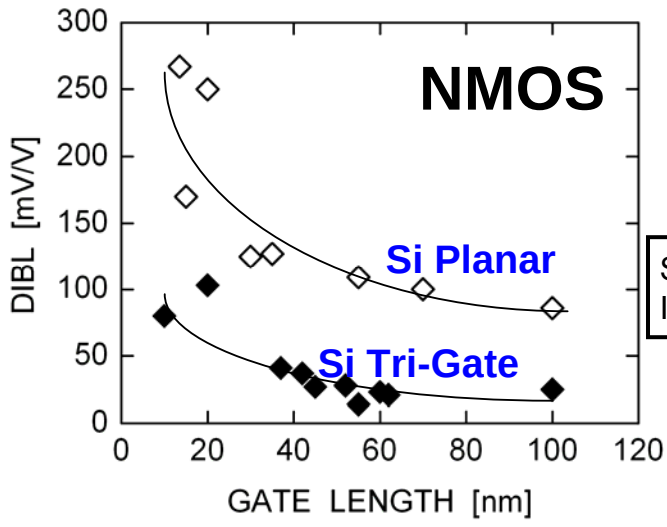


Non-Planar Double-Gate



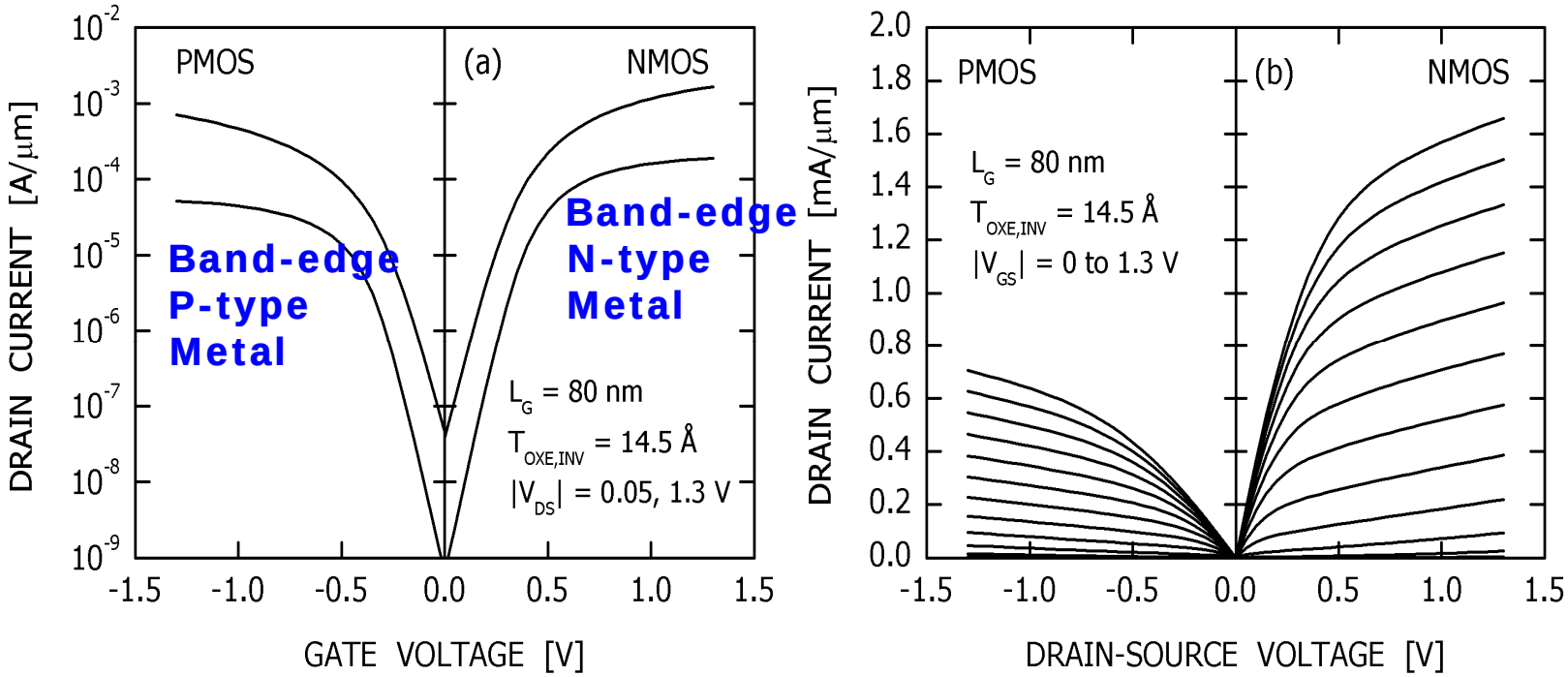
Non-Planar Tri-Gate





Source: R. Chau *et al.*, ICSICT 2004

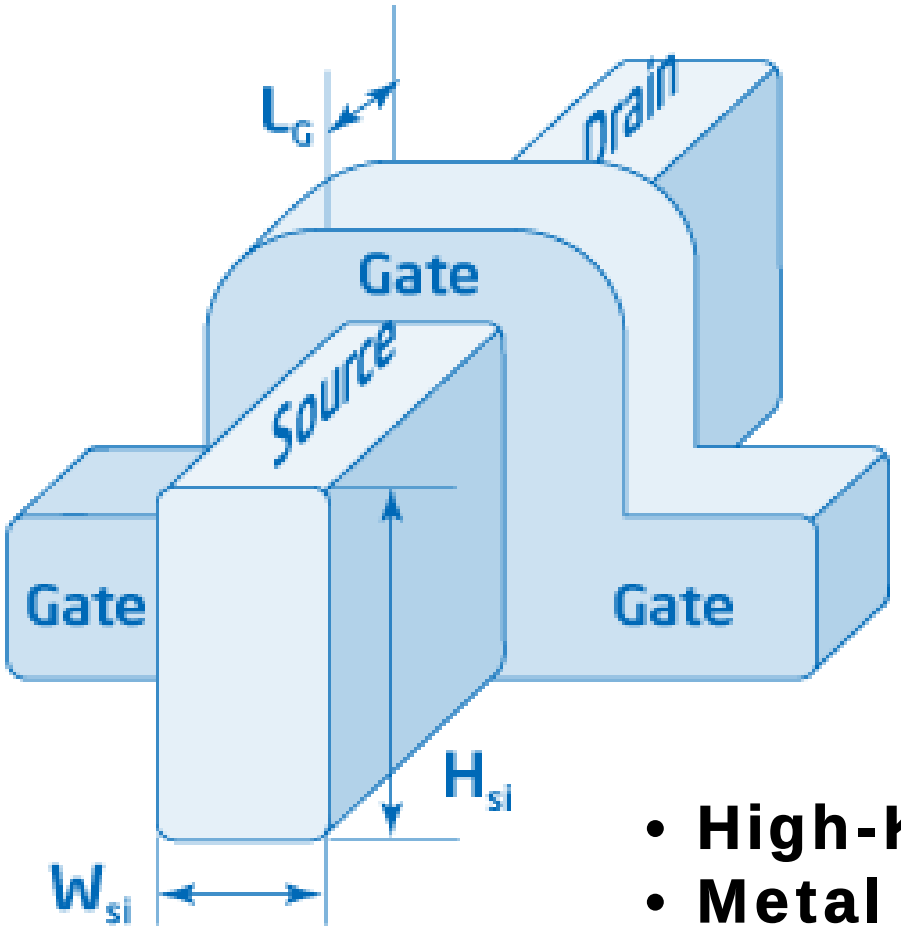
High-K/Metal Gate to Scale Toxe and Reduce Gate Leakage

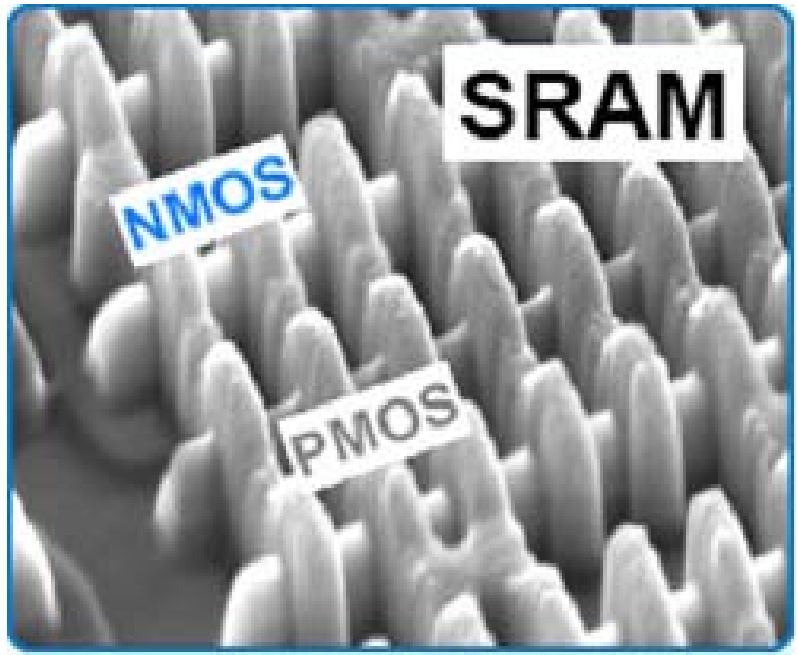


Source: R. Chau *et. al.*, IEEE EDL, Vol. 25, No. 6 , pp. 408-410, June 2004

- **Planar bulk-Si CMOS requires near band-edge p-type and n-type metal gates on high-K for "correct" transistor V_{TH}**

Tri-gate Transistor combined with *other Si Innovations*

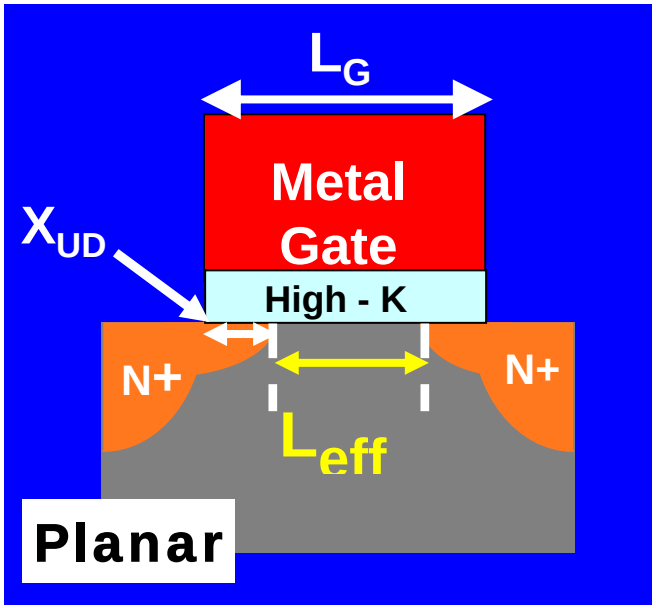


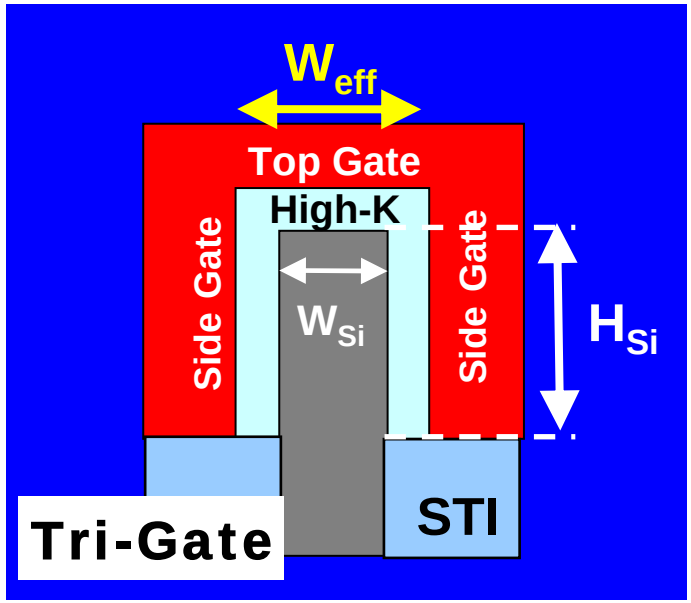


Source: VLSI 2006

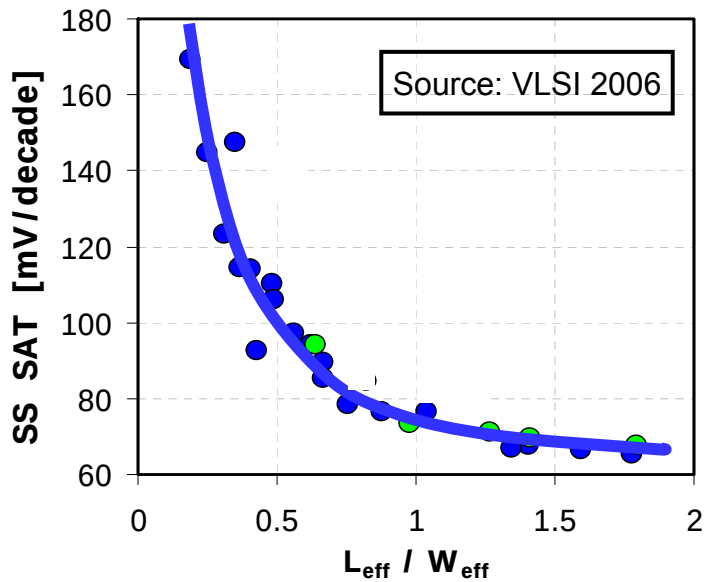
- **High-K**
- **Metal gate electrode**
- **Strain engineering**
- **Epi Raised Source / Drain**

Tri-gate Transistor Electrostatics

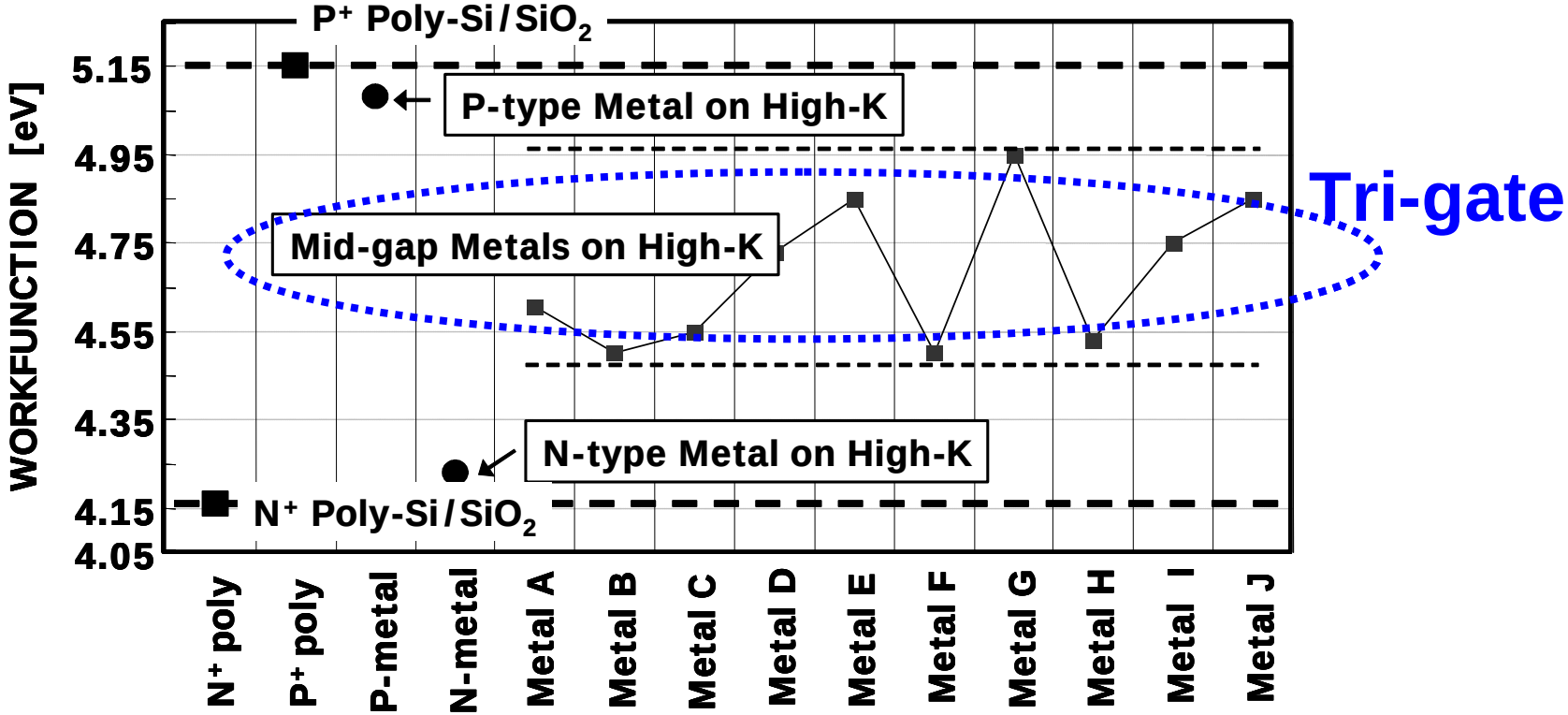




- Tri-gate electrostatics depends on the ratio of L_{eff} / W_{eff}
- Tri-gate W_{Si} scaling provides new additional knob to improve device electrostatics with L_G scaling
- H_{Si} + W_{Si} provides more raw drive current



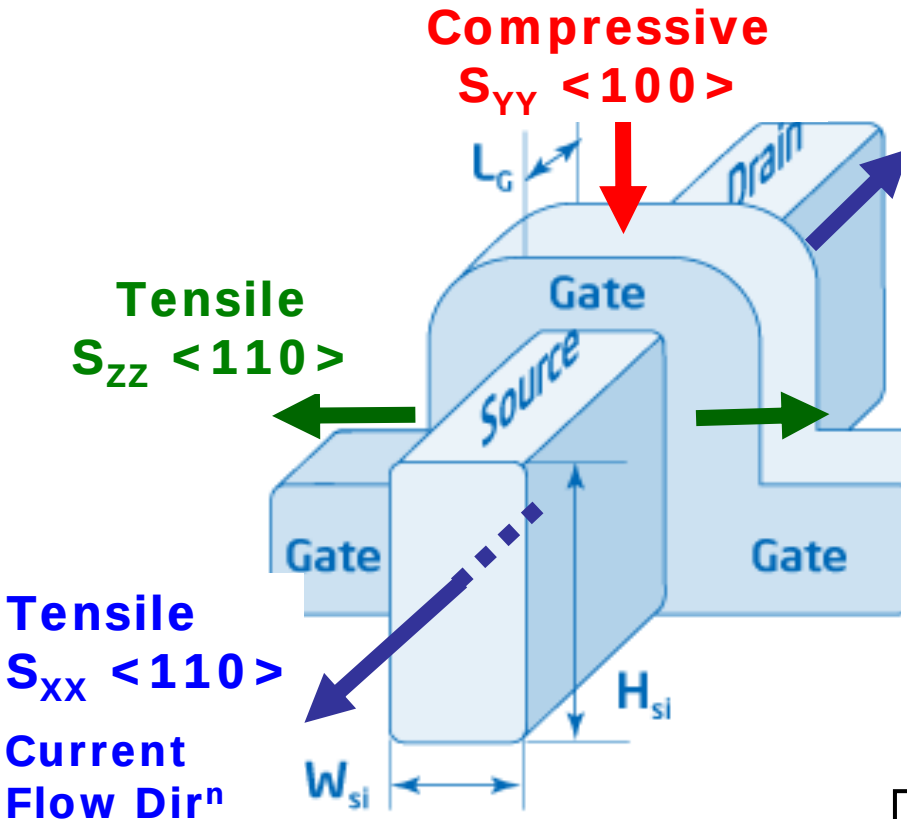
Fully-Depleted Tri-Gate Transistors allow Near Mid-gap Metal Gate Electrodes

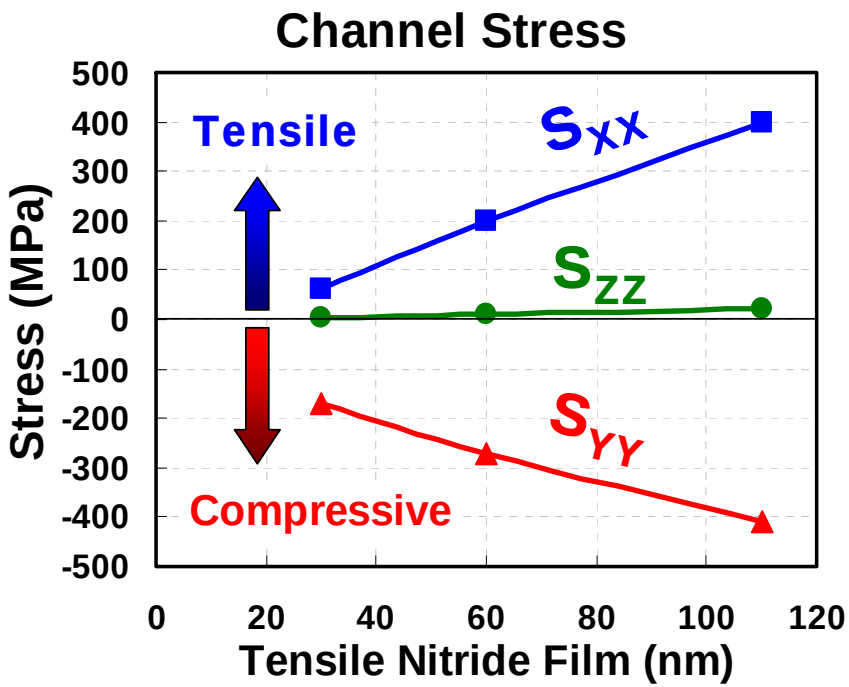


Sources:
i) R. Chau, AVS ICMI, Mar. 2004
ii) R. Chau, INFOS 2005

- **Fully-depleted Tri-gate CMOS allows i) near mid-gap metal gate and ii) low substrate doping for targeting V_{TH}**

Strain Engineering in Non-planar Tri-Gate NMOS Transistor (Tensile Nitride Film/Cap)

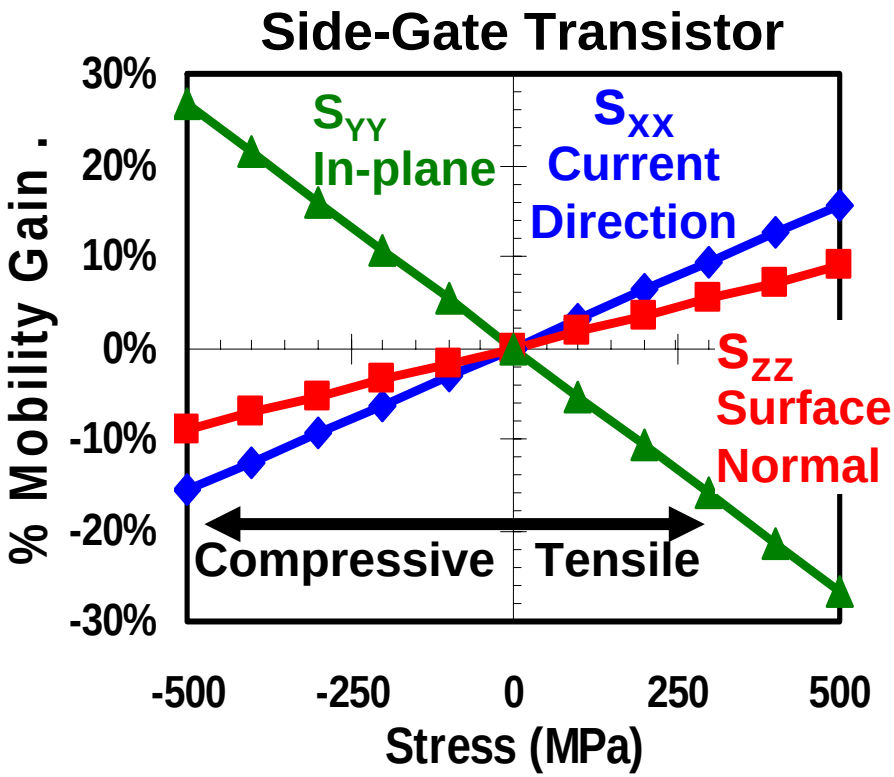


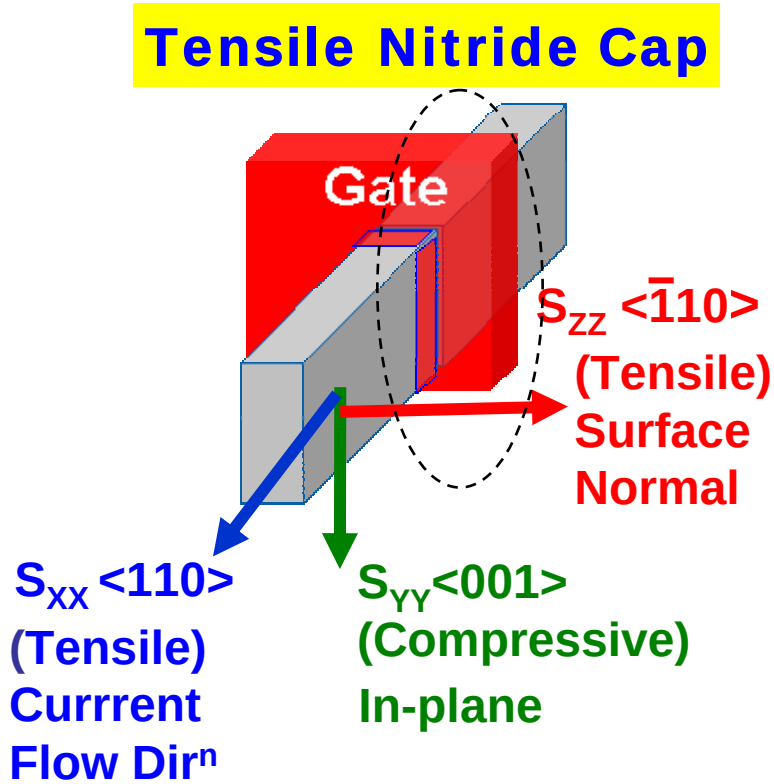


Source: J. Kavalieros, R. Chau *el al.*, VLSI 2006

- S_{XX} & S_{YY} scale with tensile nitride thickness; S_{ZZ} invariant
- S_{XX} tensile, S_{YY} compressive, S_{zz} slightly tensile

Tri-Gate NMOS Mobility vs. Strain (Side-gate)



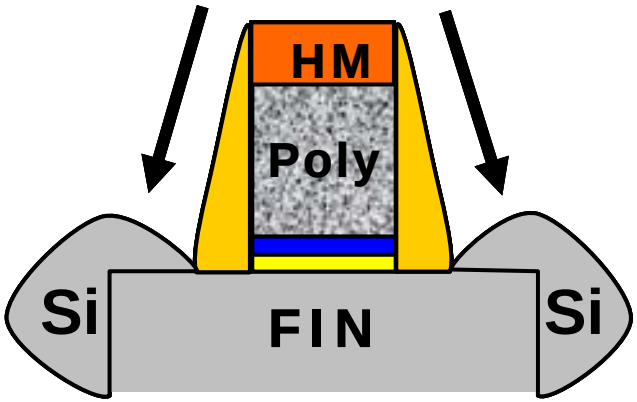


Source: J. Kavalieros, R. Chau *et al.*, VLSI 2006

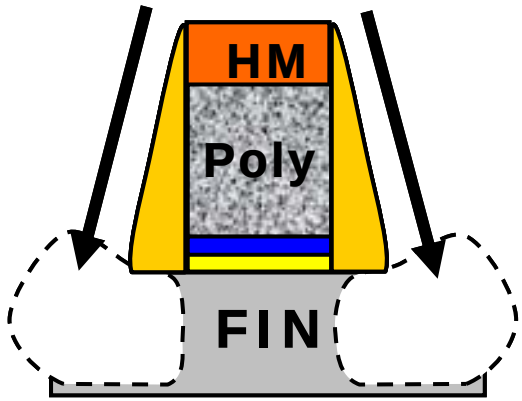
- Tensile nitride film improves side-gate mobility in tensile S_{XX}, compressive S_{YY}, and tensile S_{ZZ}
- S_{YY} (in-plane, compressive) stress has the strongest impact on side-gate mobility

Dual Epi Raised S/D for Non-planar Tri-Gate

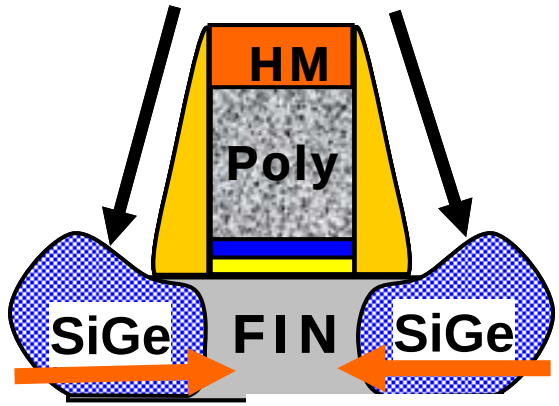
Blanket Epitaxial Si Raised S/D Growth

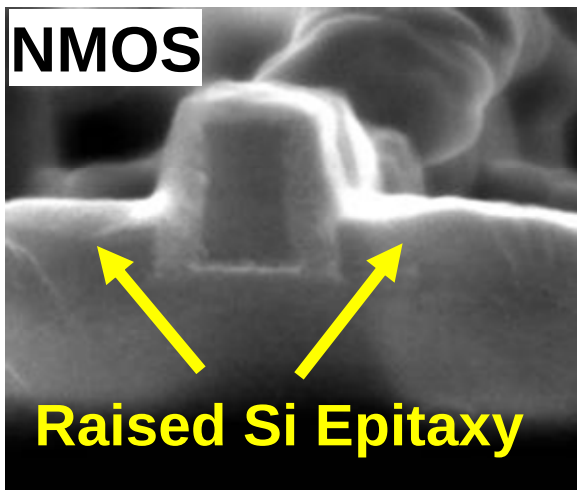


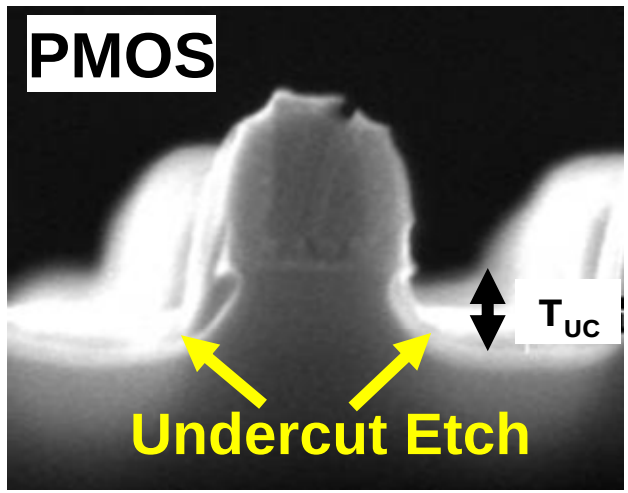
Selective Undercut Etch PMOS regions

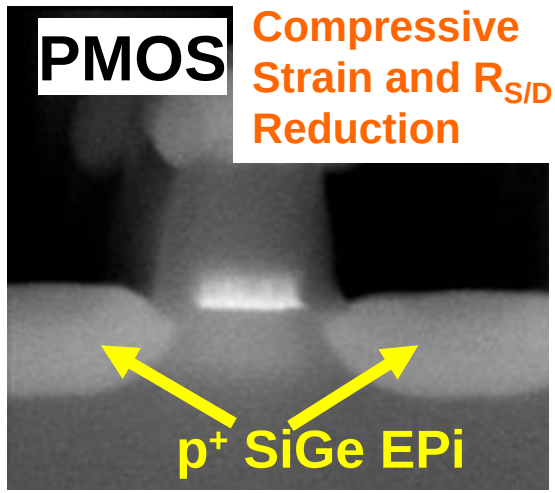


In-Situ doped p^+ SiGe Epitaxy





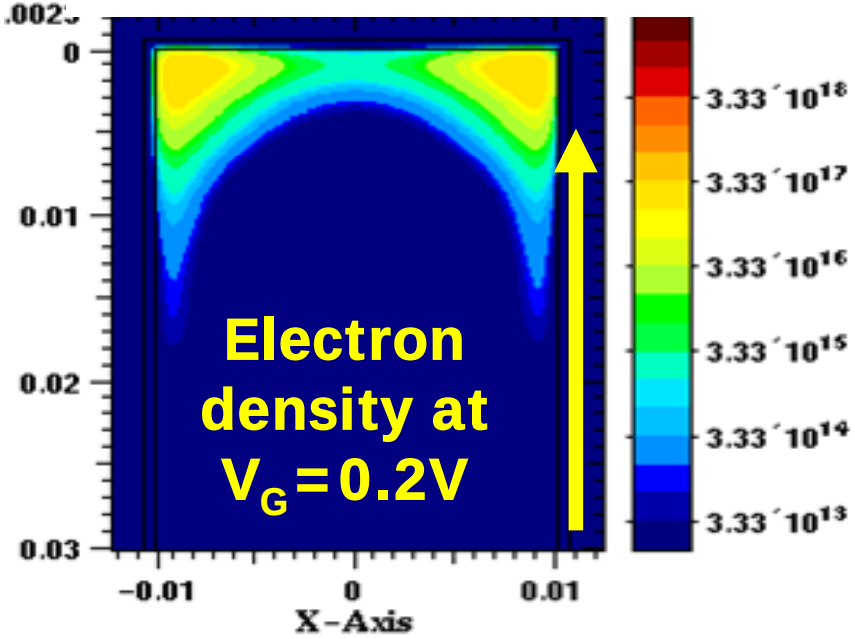




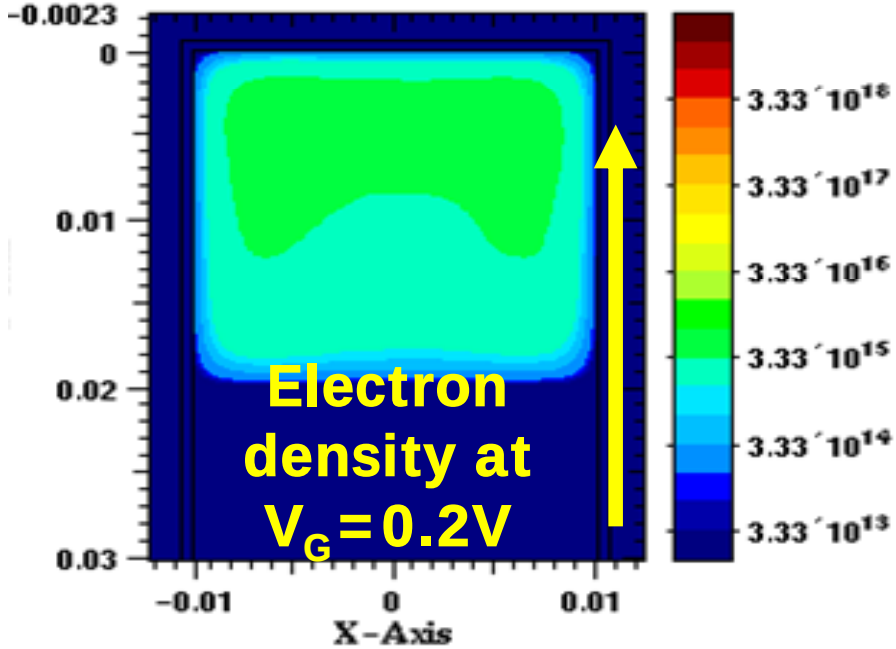
Source: J. Kavalieros, R. Chau *et al.,* VLSI 2006

Tri-Gate with High-K/MG: Non-Corner Device

Poly/SiO_2 case: High N_A



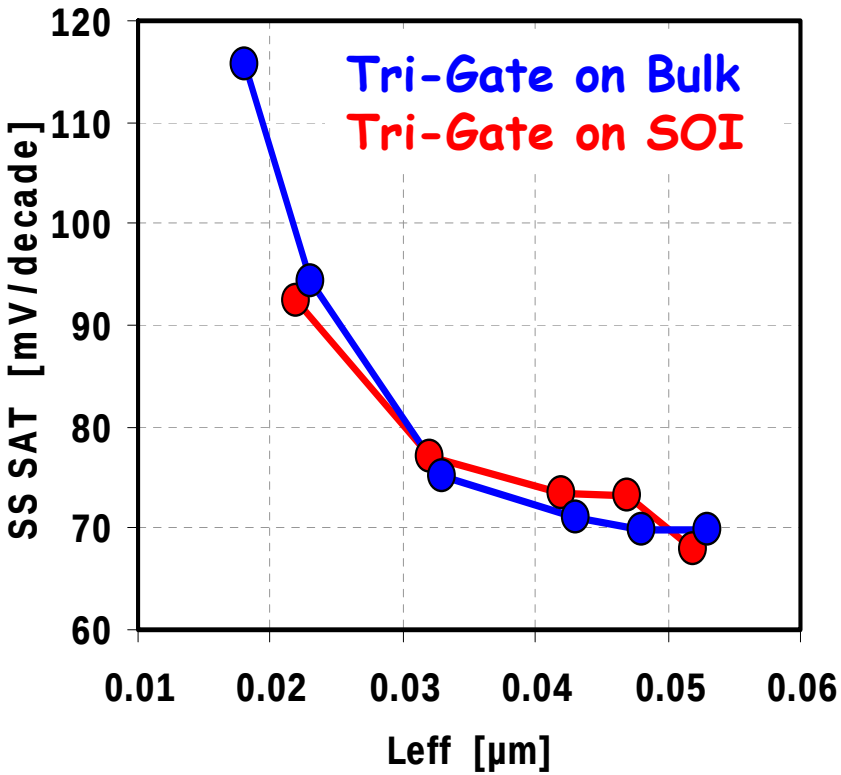
High-k / MG case: Low N_A

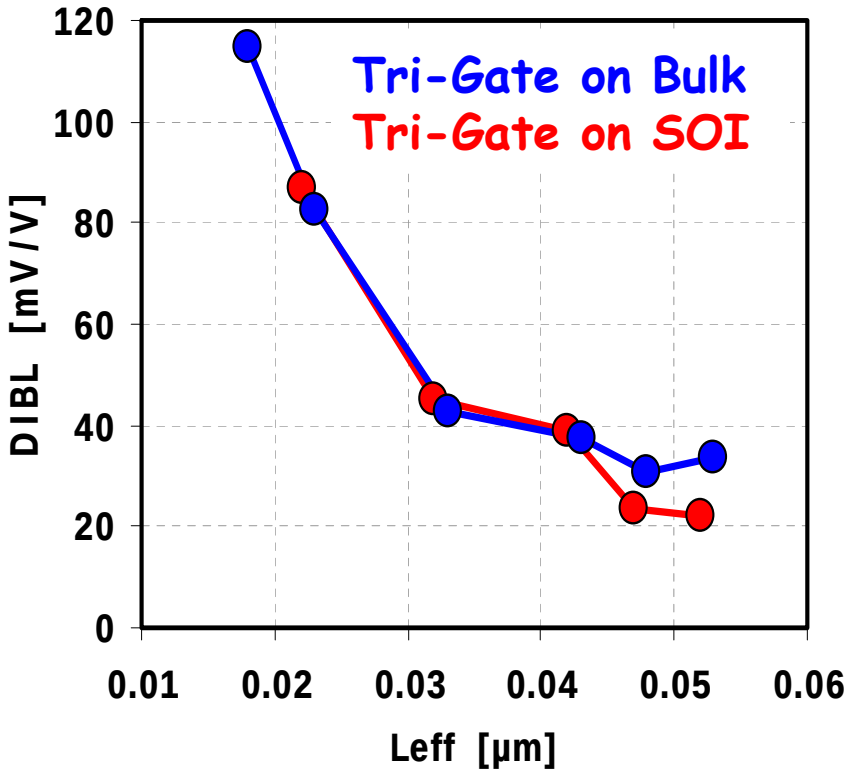


Sources:
i) B. Doyle, R. Chau *et al*., VLSI 2003
ii) J. Kavalieros, R. Chau *et al*., VLSI 2006

- **Poly/SiO2: Corner transistor is revealed at high body doping N_A**
- **Hi-K/Metal gate enables low body doping suppressing corner transistor turn-on**

Tri-Gate on Bulk Si and SOI

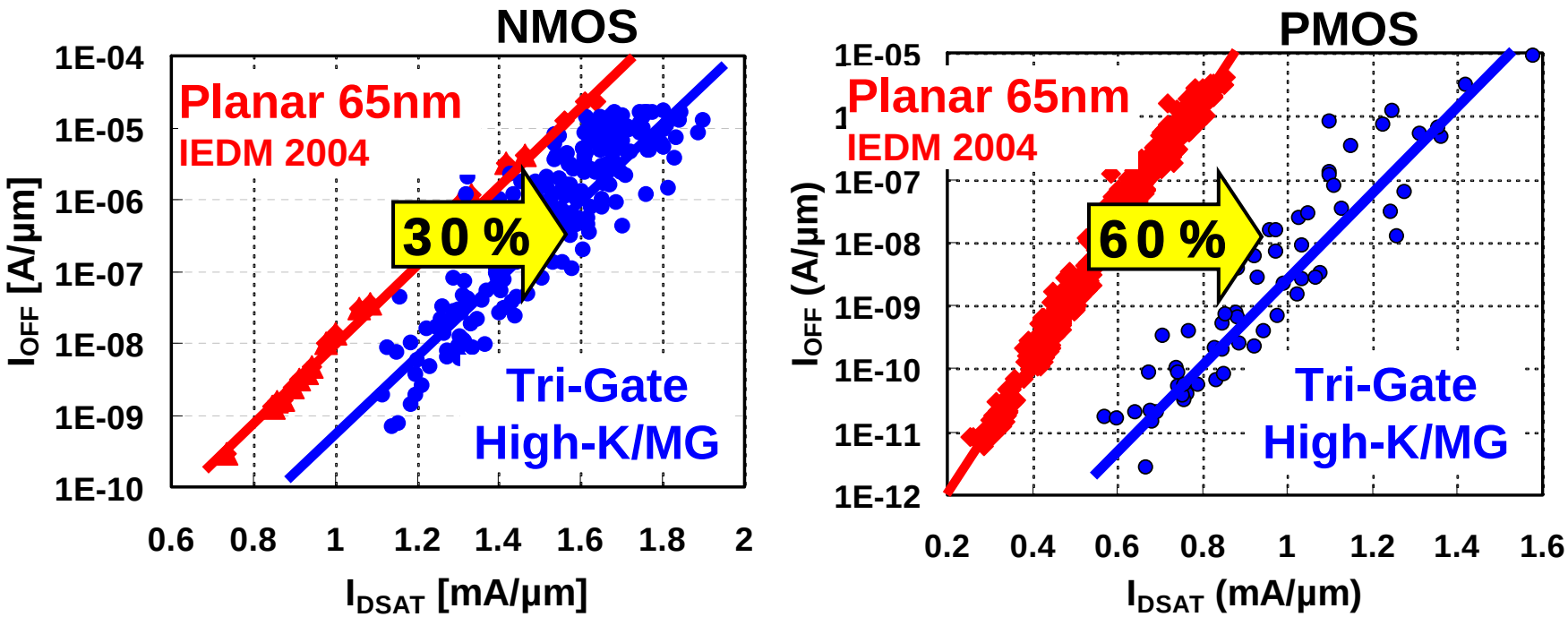




Source: J. Kavalieros, R. Chau *et al*, VLSI 2006

- **Fully depleted Tri-gate transistors have been demonstrated on both Bulk Si and SOI substrates with similar short channel performance**

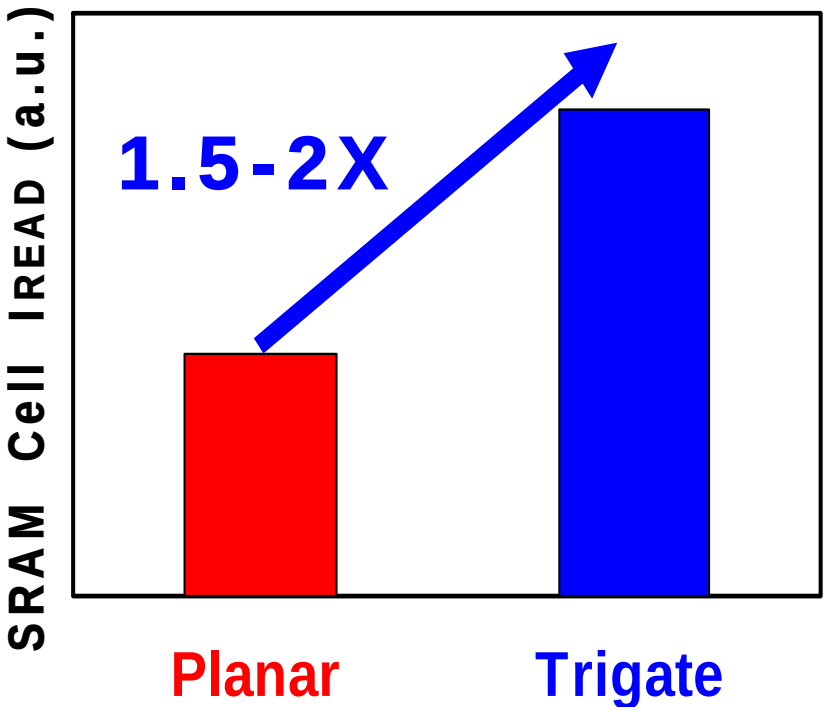
Tri-Gate CMOS on Bulk-Si



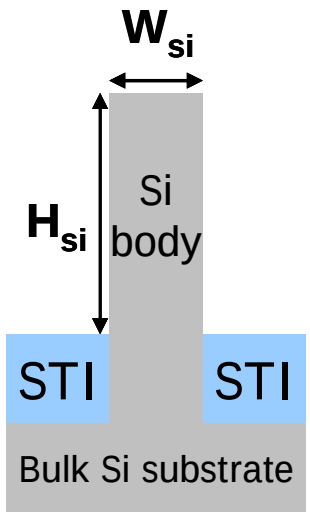
Source: J. Kavalieros, R. Chau *et al.*, VLSI 2006

- **Integrated Tri-gate CMOS on Bulk-Si with i) high-K ii) metal-gate, iii) strained silicon and iv) dual Epi raised source and drain**

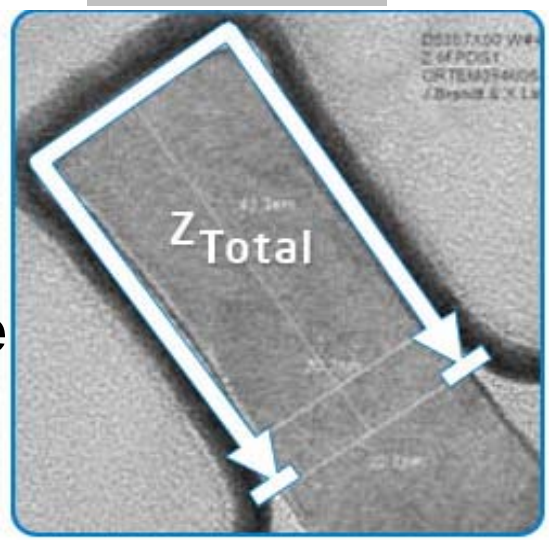
Tri-gate SRAM Cell



Tri-Gate transistor width
= $2*H_{si} + W_{si}$

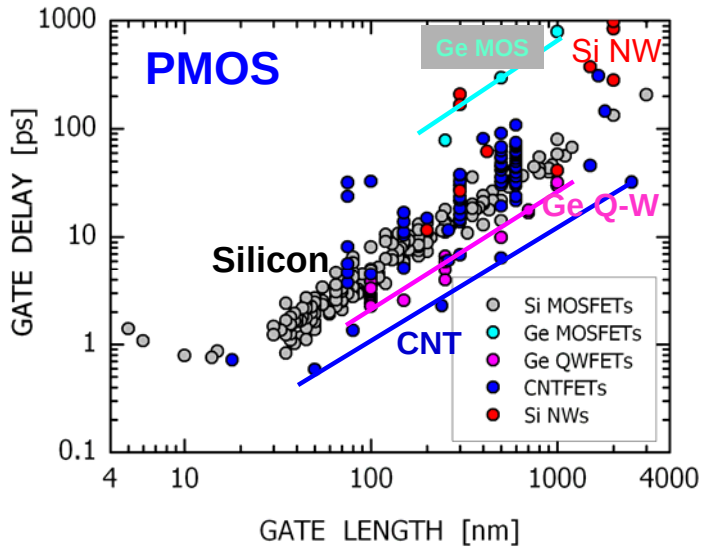


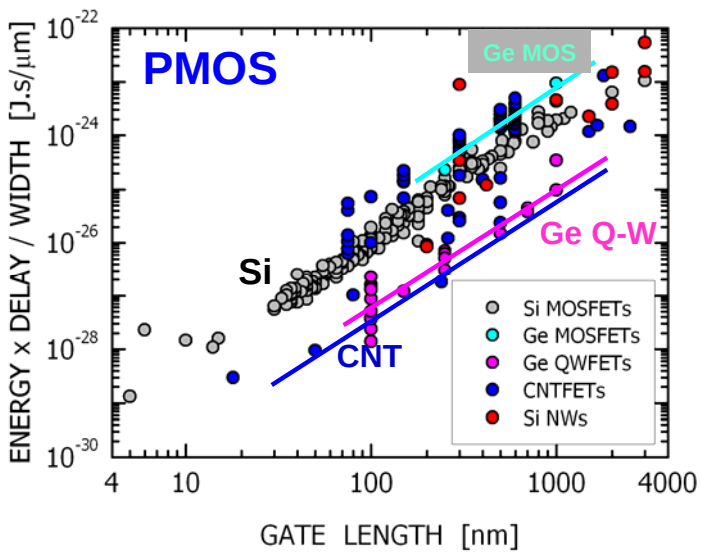
Sources:
i) J. Kavalieros, R. Chau *et al.*, VLSI 2006
ii) R. Chau, Technology@Intel Magazine, Aug. 2006

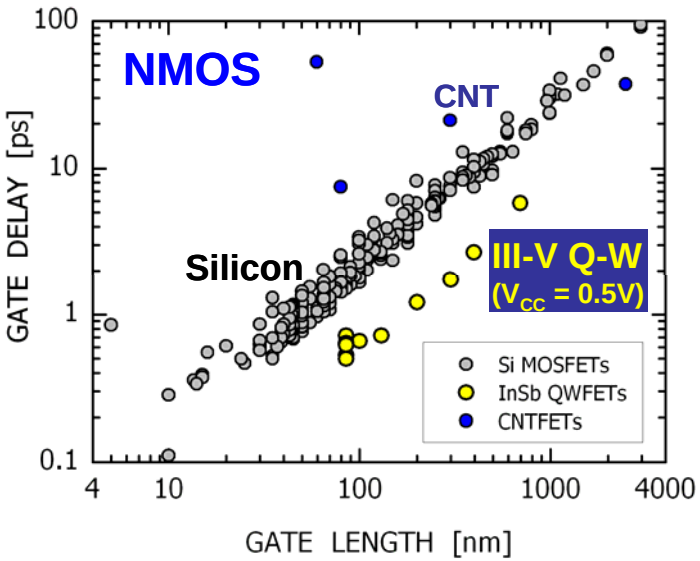


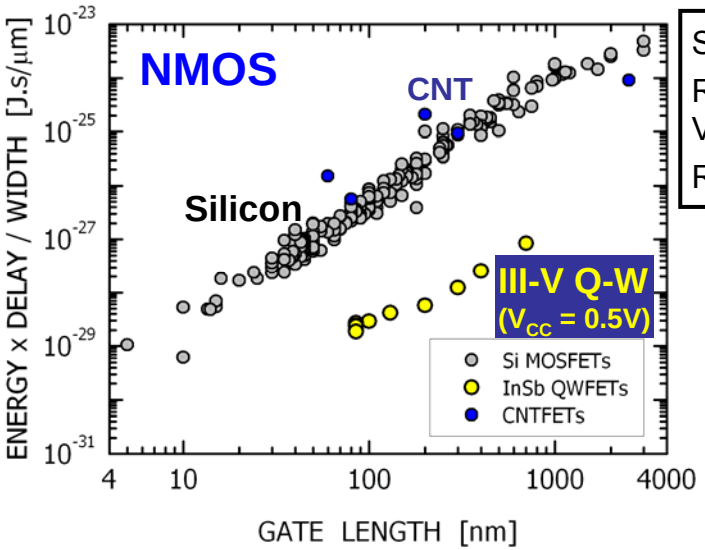
- **For the <u>same</u> SRAM cell size, the Tri-gate device has more device width than the planar device, hence higher cell read current**

Emerging Non-Si Device Research: Required Benchmarking







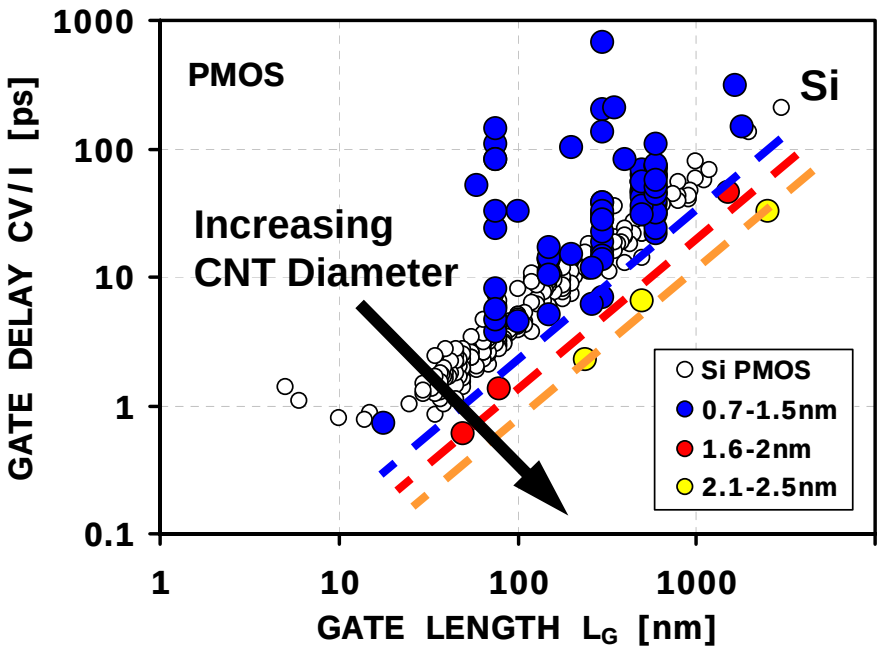


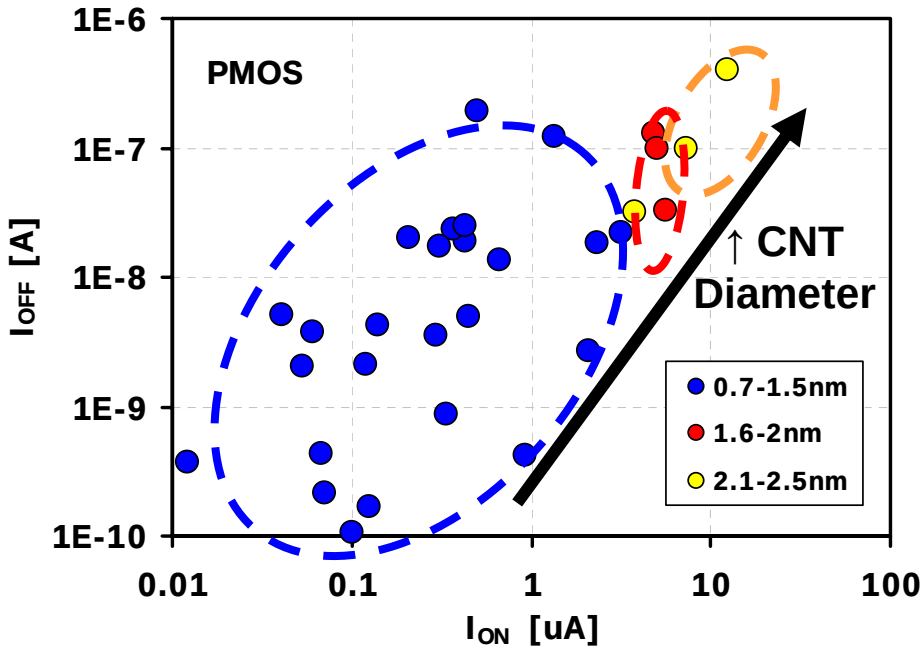
Sources:

R. Chau *et al*., IEEE VLSI-TSA, 2005

R. Chau, DRC 2006

Emerging Device: Carbon Nanotube Transistor

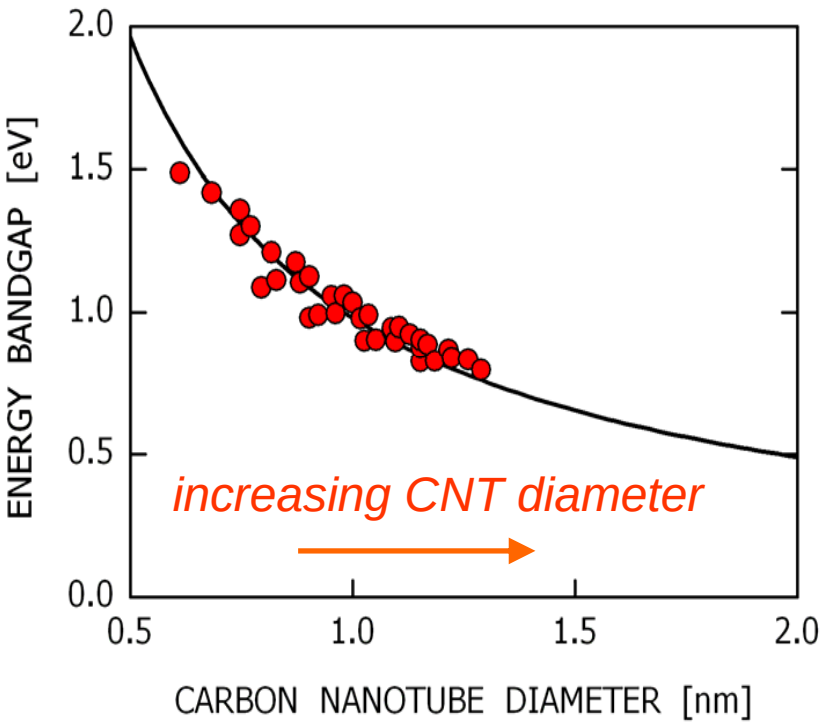


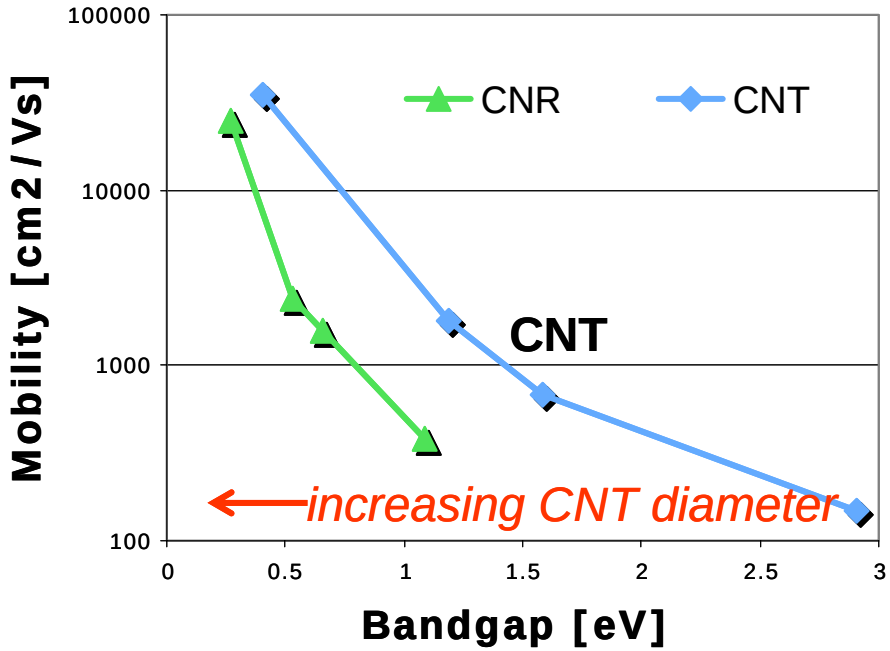


Source: R. Chau, DRC 2006

- **Device performance of CNT depends on tube diameter**
- **High-performance of CNT may come at the expense of high device off-state leakage (energy band gap related)**

Emerging Device: Carbon Nanotube Transistor

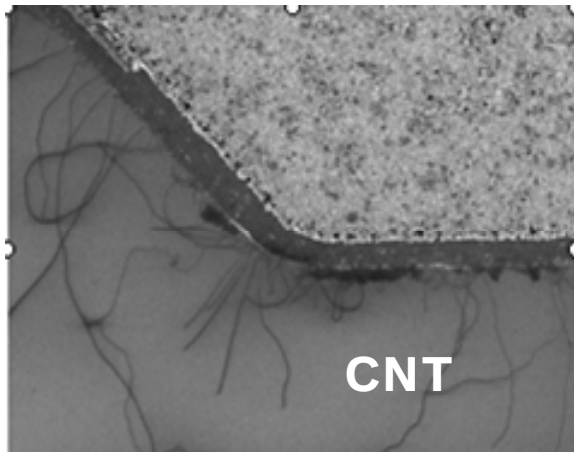


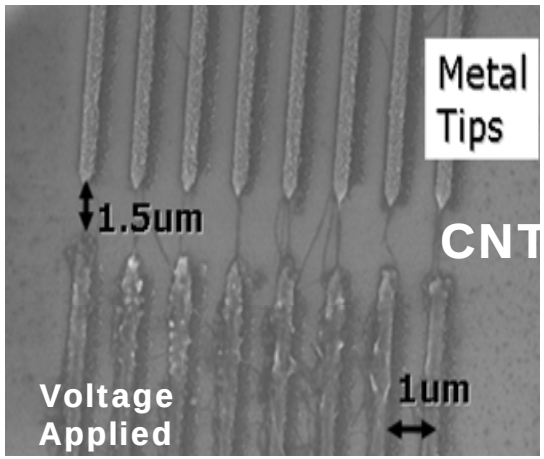


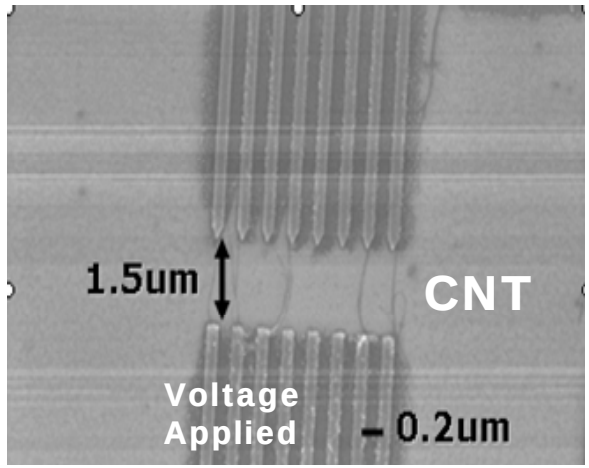
Source: B. Obradovic, R. Kotlyar, *et al*, Applied Physics Letters, 88, 142102 (2006).

- **Performance and leakage related to CNT diameter, which is related to energy band gap**
- **Analogous to low-bandgap/high-mobility III-V devices which require quantum-well device structures (?)**

Fundamental Issue for CNT: Assembly Problem



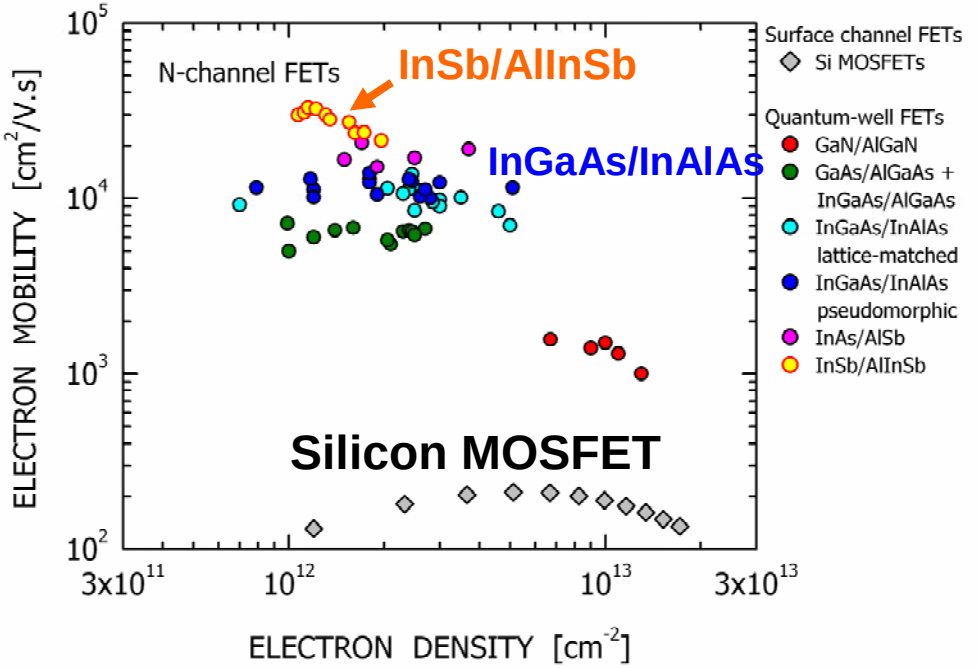


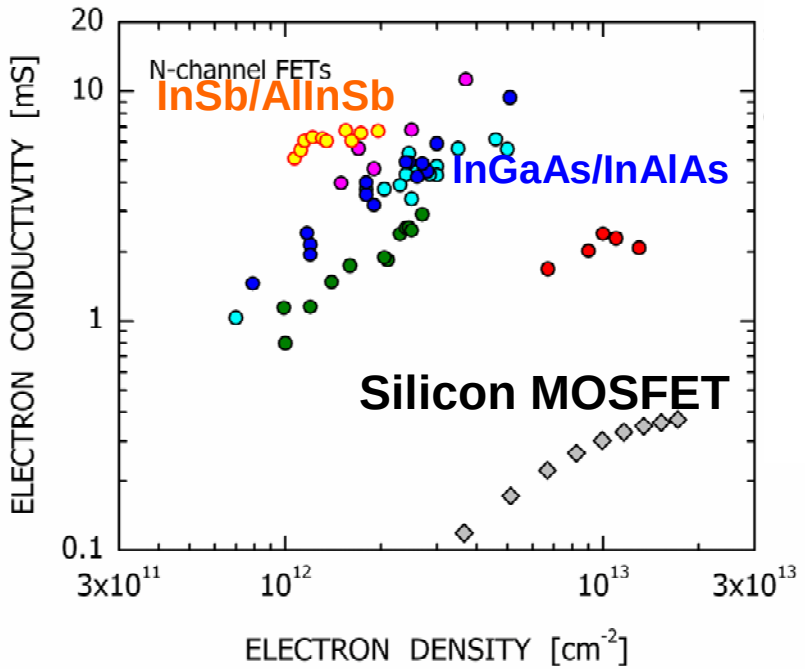


Source: R. Chau, DRC 2006

- **Good progress has been made in assembling bottom-up chemically synthesized electronic materials (e.g. CNT)**
- **However, still many problems to solve before transistor arrays can be made for VLSI applications**

Why III-V Research for Future Logic Applications?

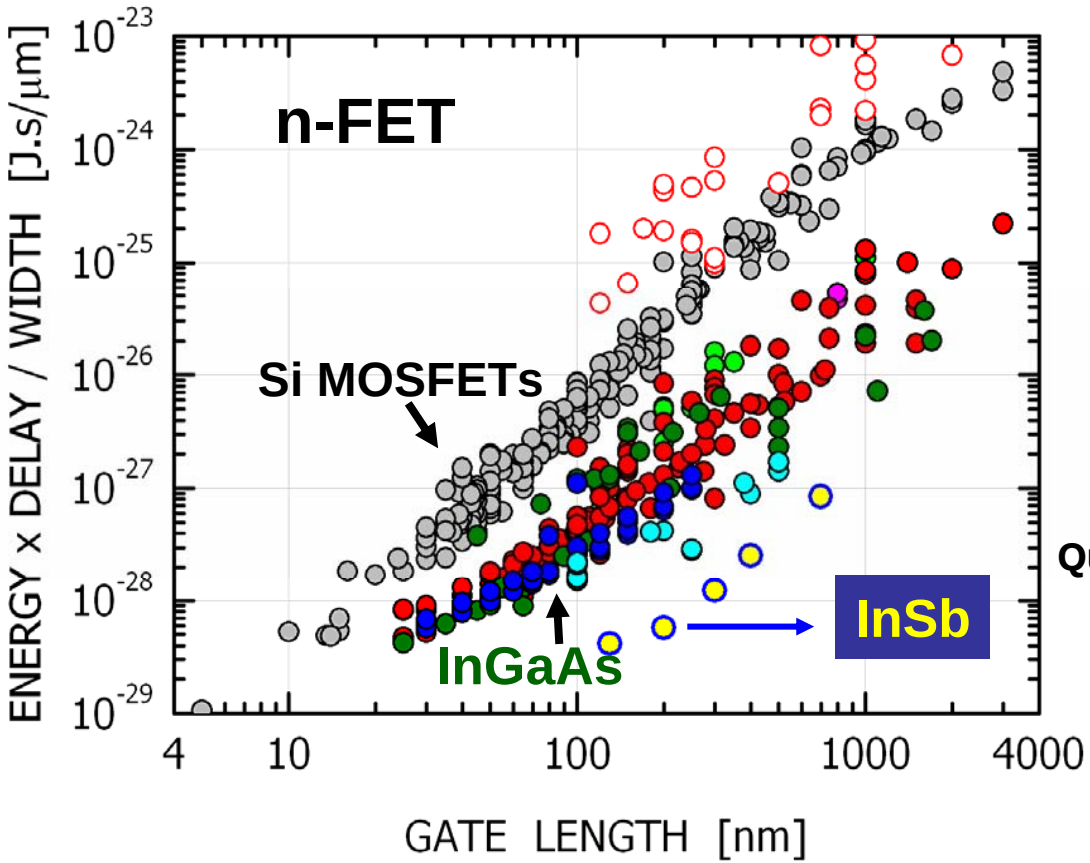




Source: R. Chau *et al.*, CSICS 2005

- **III-V has been used in commercial communication & optoelectronics products for a long time**
- **III-V quantum-wells show ~100X higher electron mobility and ~20X higher electron conductivity than Si ➔ [potentially high-speed + low-power]**
- **Top-down patterning as opposed to bottom-up chemical synthesis**

III-V Nanoelectronics: Low Energy-Delay Product



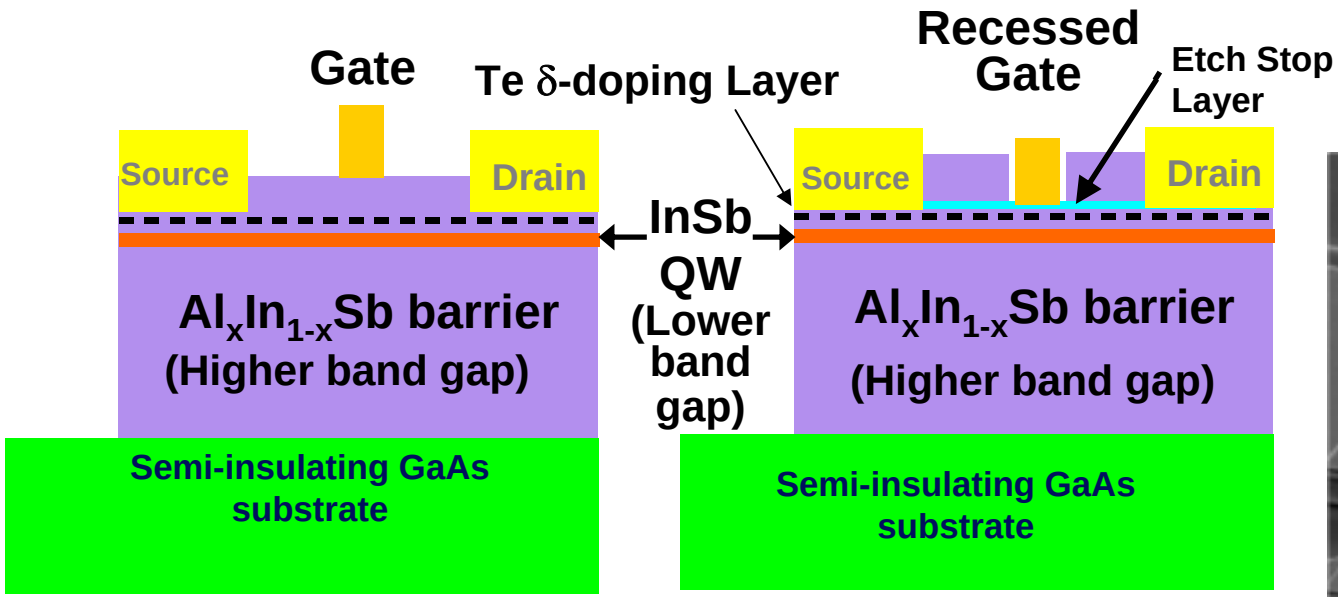
	QW Bandgap
Si MOSFETs	
GaN/AlGaN	3.4eV
GaAs/AlGaAs LM	1.4eV
InGaAs/AlGaAs PM	1.1-1.25eV
InGaAs/InAlAs LM	0.8eV
InGaAs/InAlAs PM	0.55-0.75eV
InAs/InGaAs/InAlAs PM	0.36/0.8eV
InAs/AlSb PM	0.36eV
InSb/AlInSb	0.18eV

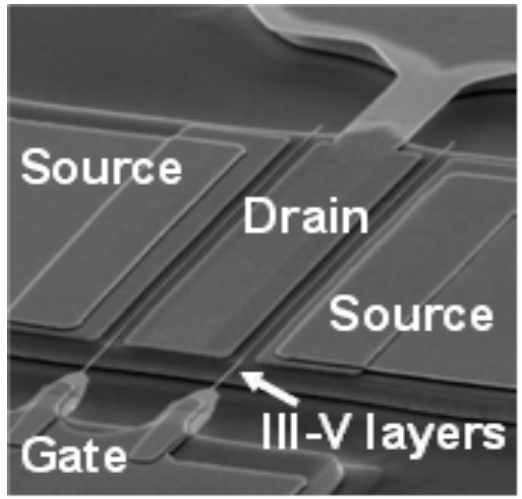
Quantum-well / Barrier

Source: R. Chau *et al.*, CSICS 2005

- **Of all the III-V quantum-well systems, InSb QW has the lowest energy-delay product [highest electron mobility, lowest band gap, lowest V_{CC} (0.5V)]**
- **InGaAs QW is also important for low V_{CC} (0.5V-0.7V)**

Example of III-V Quantum-Well (QW) Transistor





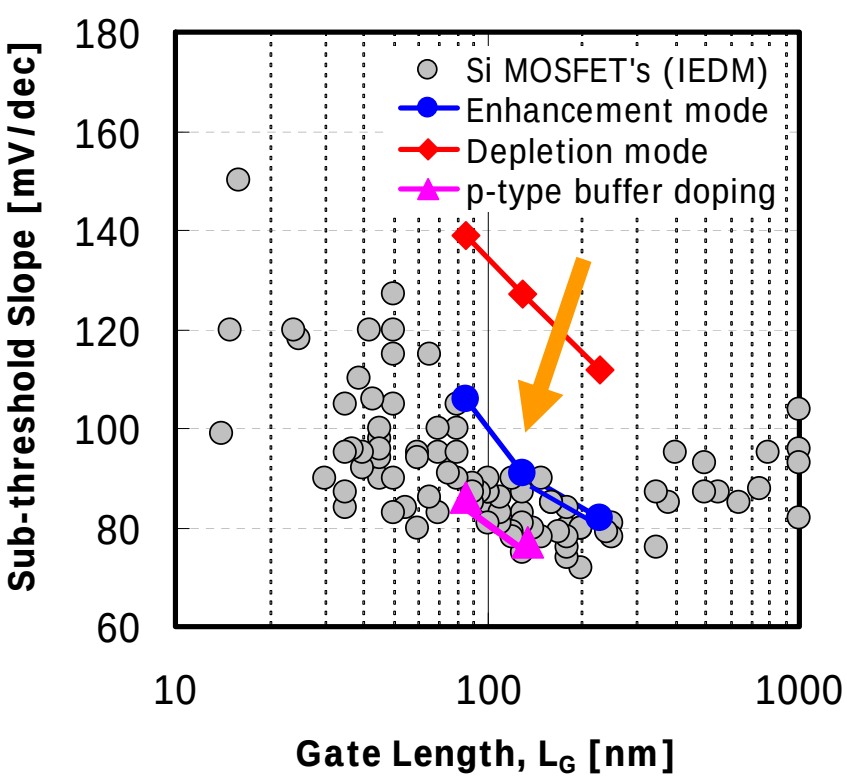
Depletion mode (Normally ON)

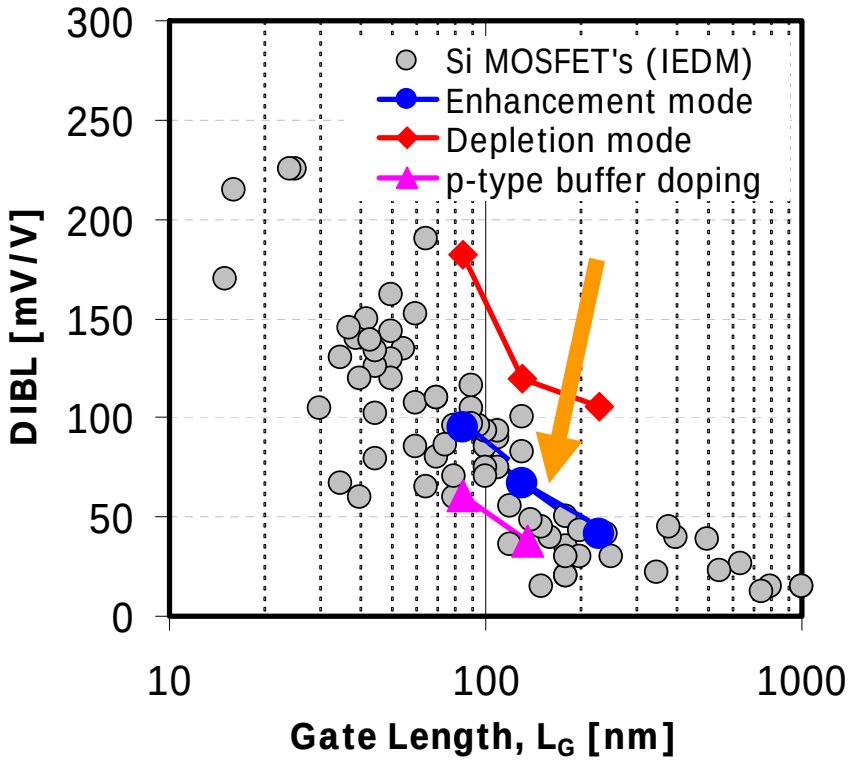
Enhancement mode (Normally OFF)

Source: Intel and QinetiQ
ICSICT 2004, IEDM 2005

- **Quantum-well to reduce parasitic junction leakage and I_{OFF}**
- **At present Schottky metal gates are used without gate dielectric …… high parasitic gate leakage current**

Scalability of Quantum-Well Transistors

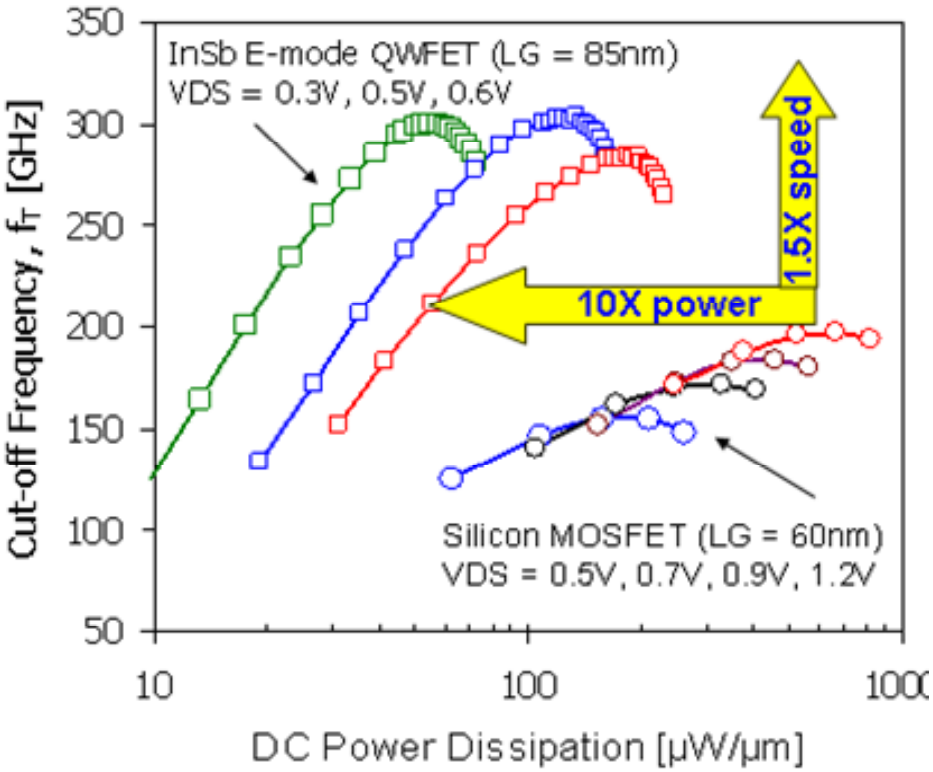


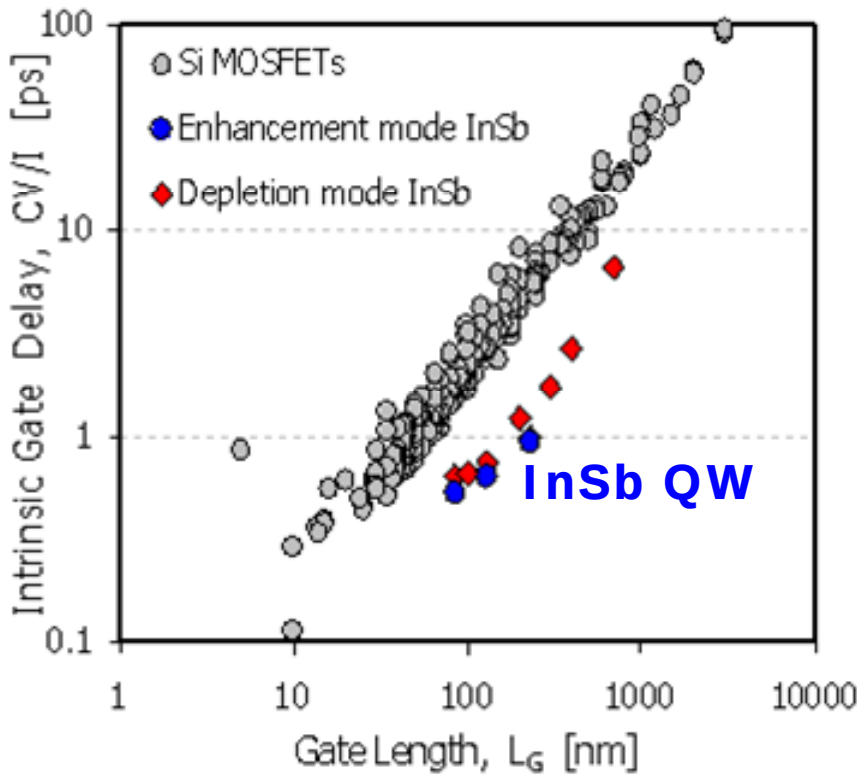


Source: Intel and QinetiQ, IEDM 2005

- **III-V QW transistors can achieve similar subthreshold slopes and DIBL to standard Si MOSFETs**

Potentially Useful for Future High-Speed and Low-Power Applications

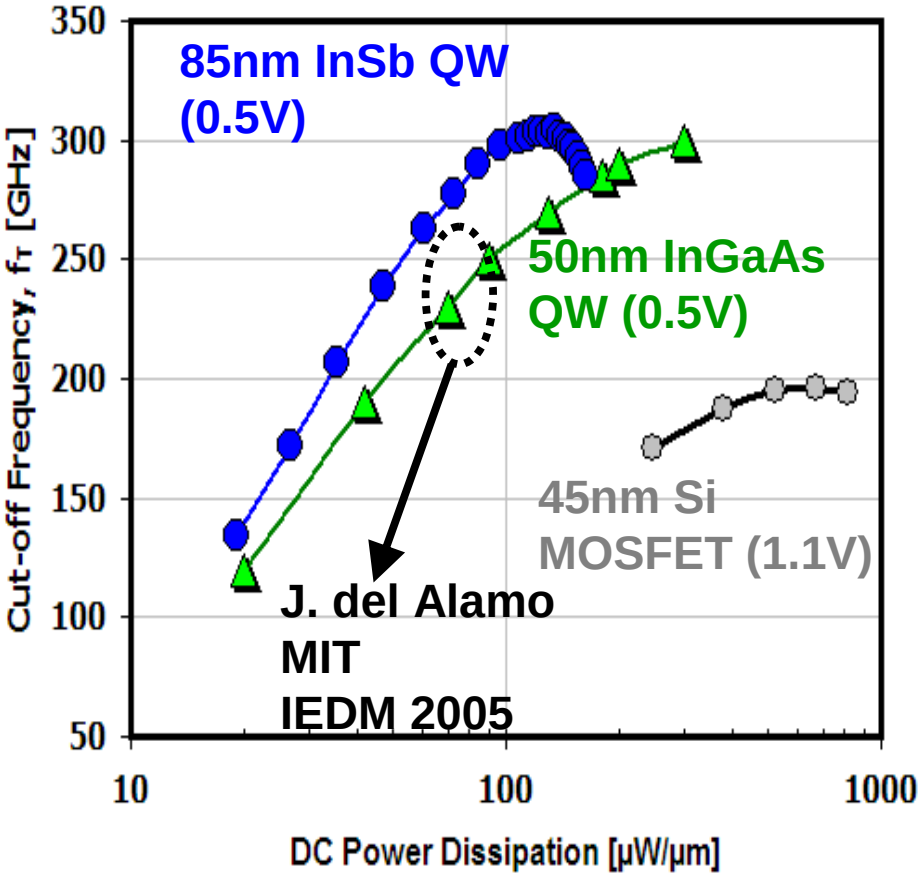


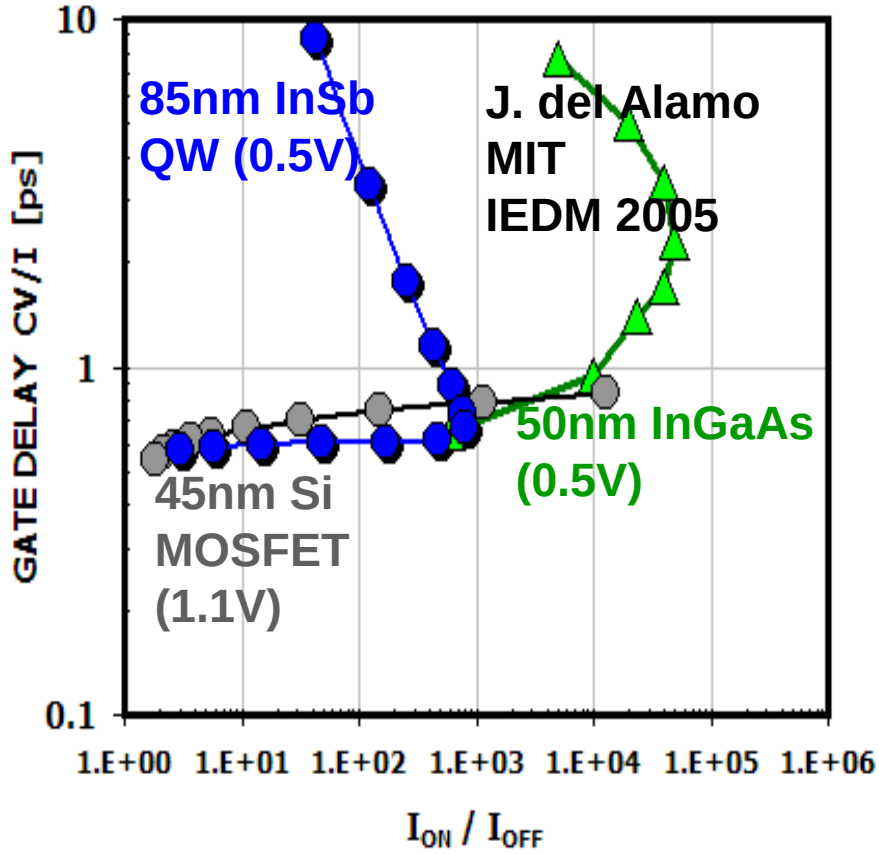


Source: Intel and QinetiQ, IEDM 2005

- **InSb QW shows high performance at low V_{CC} (>300 GHz at 0.5V)**

Potentially Useful for Future High-Speed and Low-Power Applications





Source: R. Chau, DRC 2006

- **InSb QW has the highest performance because of the highest mobility; InGaAs QW also shows high performance at 0.5V**

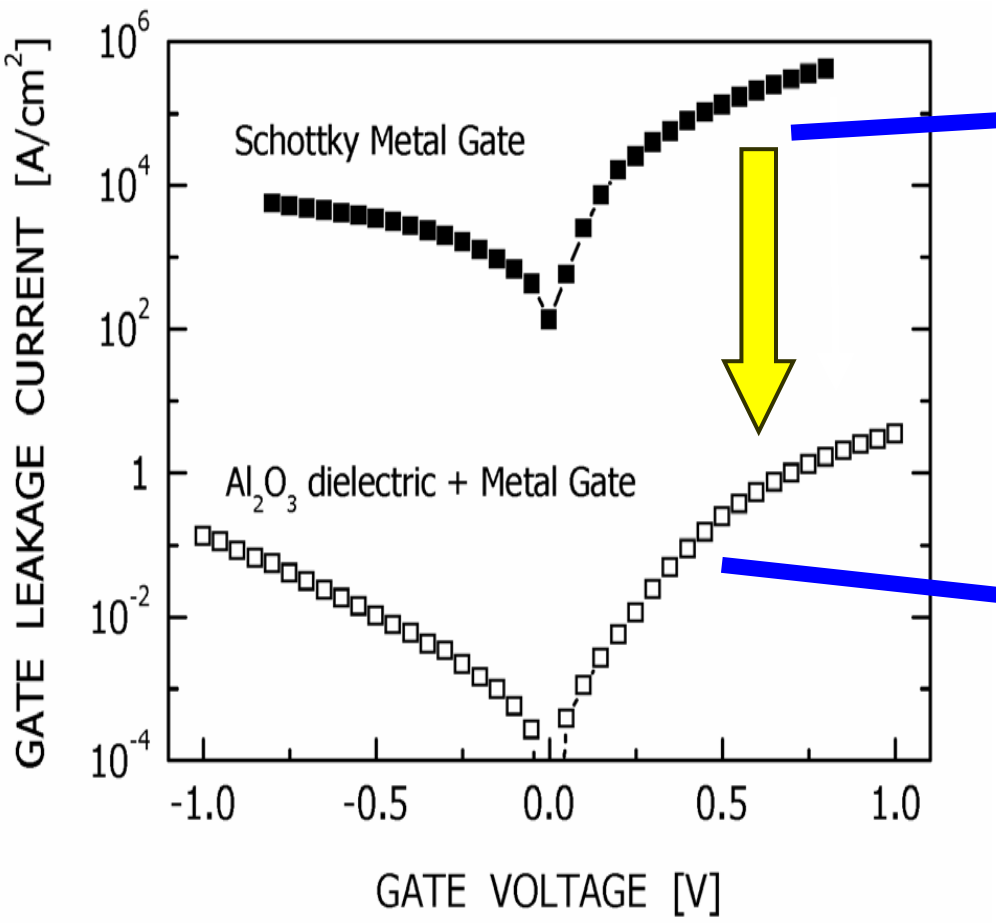
III-V Challenges

- Stable and reliable gate dielectrics for III-V
- Integration of III-V on Si
- PMOS solution to the CMOS configuration

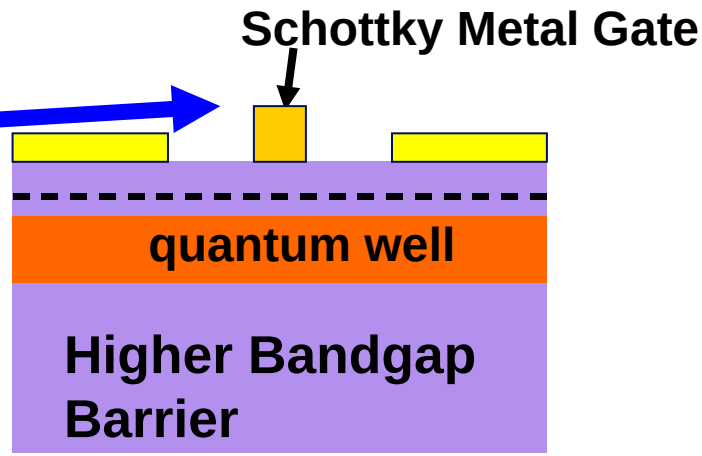
III-V Opportunities

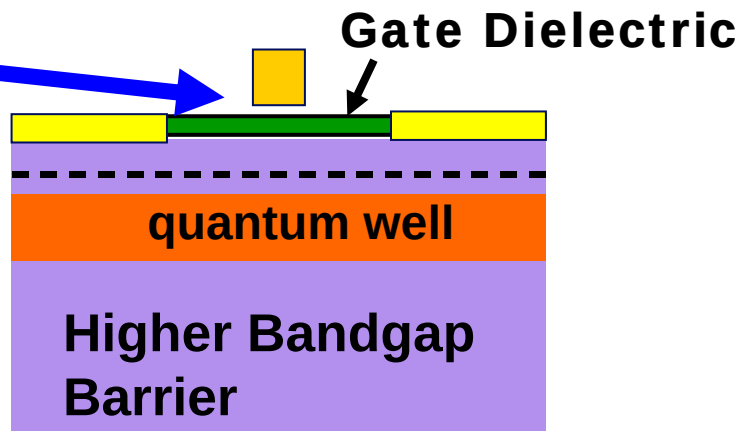
- Very high-speed circuits at low supply voltage (e.g. 0.5V) for future computation applications
- III-V on silicon to enable new functionalities on silicon and also new applications

Parasitic Gate Leakage due to Schottky Gate



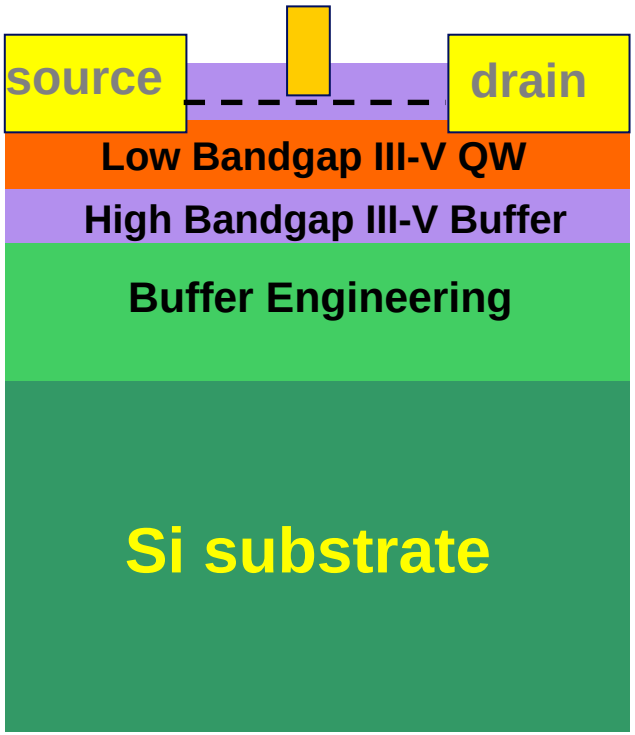
Source: Intel and QinetiQ, IEDM 2005

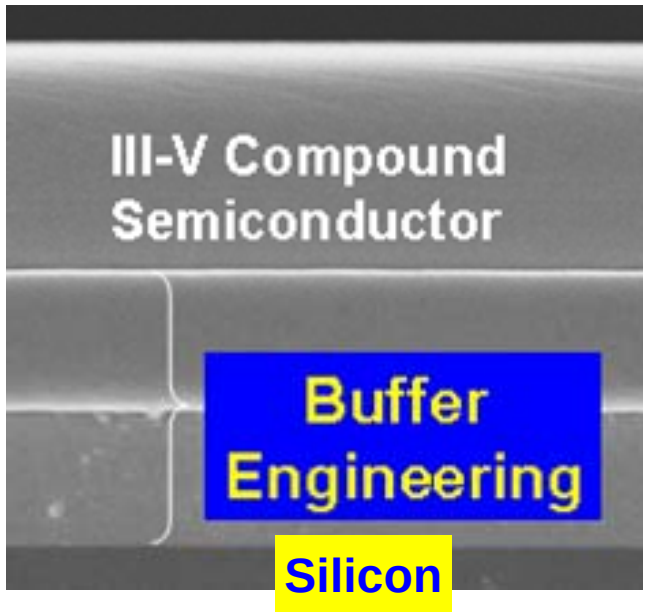




- **Gate dielectric required to reduce the parasitic gate leakage**

Integration of III-V on Si





- **Issues/Challenges**
  - **Large lattice mismatch**
  - **Polar/non-polar mismatch → anti-phase domain**
  - **Thermal mismatch**

SUMMARY

- **Through Si innovations, Si CMOS transistor scaling and performance trends will continue well into the next decade**
- **More non-Si electronic materials and technologies will be integrated onto Si to enable future high-speed and low-power computation, as well as adding new functionality and new applications**
- **Emerging nanotechnologies present both challenges and opportunities for future VLSI applications**